UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/736,353	12/14/2000	William L. Betts	061607-1360	8924

7590 10/31/2005

SCOTT A. HORSTEMEYER
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L. L. P
100 GALLERIA PARKWAY, SUITE 1750
ATLANTIC, GA 30339-5948

EXAMINER	
CORRIELUS, JEAN B	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/736,353	BETTS, WILLIAM L.	
	Examiner	Art Unit	
	Jean B. Corrielus	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/26/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31 and 34-51* is/are pending in the application.

4a) Of the above claim(s) *35-48* is/are withdrawn from consideration.

5)☒ Claim(s) *17-22* is/are allowed.

6)☒ Claim(s) *1-16,23-31,34 and 49-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-31 and 34 in the reply filed on 9/26/05 is acknowledged.

2. In the last office action, claims 49-51 were inadvertently indicated to be directed to a receiver/decoding while the claims were directed to a transmitter and/or encoding technique. Claims 49-51 now join the elected group of invention (group I), namely claims 1-31 and 34 and claims 35-48 (group II) are non-elected.

3. Claims 35-48 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on 9/26/05.

Specification

4. The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code. Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

5. The disclosure is objected to because of the following informalities: page 21, line 23, the sentence "interleaver of the" is incomplete.

Appropriate correction is required.

Drawings

6. The drawings are objected to because fig. 3 and fig. 5, the middle circuit coupled to the adder 304, "301" should be "302" and fig. 4 "4017" should be "407". In addition, the drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 305, shown in fig. 3 and in fig. 5.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

7. Claims 8, 28-31 and 34 are objected to because of the following informalities: claim 8, line 1, what does it mean by "bits on tones"? Claim 28, line 4, "capable of" should be replaced by "for"; line 9, "the first" should be replaced by "a first one" in both occurrences; line 10, "connected" should be replaced by "first one of the"; line 11, "encoder" should be "encoders"; line 12, "the second" should be replaced by "a second one" in both occurrences; line 13, "connected" should be replaced by "second one of the"; line 14, "encoder" should be "encoders"; line 15, "a" should be inserted after "connecting"; line 15, before "inputs", "one of the remaining"; line 15, "the successive" should be replaced by "a successive one of the remaining" ;line 16, "connected" should be replaced by "the successive one of the remaining"; line 16, "encoder" should be "encoders". Claim 34, line 1, recites a transmitter comprising". It appears that "transmitter" should have been "interleaver" or "encoder"; lines 7-8, what does it mean by " a third bit based on ... **the logic gates**"? Claim 34, line 5, "inputs" should be "input" so as to be consistent with antecedent in line 2. The same comment applies to line 7. Note that any claim whose base claim is objected is likewise objected. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 49-51 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 49 recites the limitation of "outputting the plurality of encoded bits to a constellation buffer **in the first sequence**". However, the specification as filed does not provide support for such limitation as claimed. The specification teaches at most the skipping switch output the encoded bits to a constellation buffer in non-sequential manner, see page 19, lines 23-25 and page 21, lines 1-15. Claims 50 and 51 are similarly rejected.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Betts et al US Patent No. 4,677,625 in view of Maloon et al US Patent No. 4,635,278.

Betts et al discloses a transmitter (fig. 1), comprising: a series of trellis encoder 18-24 for receiving a plurality of bits and for outputting a encoded plurality of bits; (note

that the trellis encoders are a type of convolutional encoder see for instance abstract, where convolutional decoder and trellis decoder are used interchangeably) and (b) a synchronized dual switch (10, 16 and 42) functionally equivalent to the claimed synchronized dual skipping switch configure to pass the plurality of bits to the trellis encoder (convolutional encoder) in a non-sequential order and outputting the trellis (convolutionally) encoded plurality of bits in the non-sequential order. Note that prior to providing the bits to switch 16, the sequential data stream is scramble in randomizer 10 so as to change the order of the data sequence, hence the signal output by switch 42 is not sequential. See col. 2, lines 22-25.

However, Betts et al does not teach that each data bit includes a tone. Maloon teaches a method for transmitting digital signal in which one or two tone is selected for each bits see abstract. Given that fact, it would have been obvious to one skill in the art to incorporate such a teaching in Betts et al so as to improve data encoding and decoding. See for instance Maloon et al, abstract, lines 1-14.

As per claim 2, note that Betts et al further teaches a QAM encoder (mapper) that maps the inputs signal into a point of a preselected signal constellation see col. 2, lines 55-60. It fails to however teach that the mapper (QAM encoder maps the input bits to a two points constellation. As acknowledged by applicant at page 19, lines 20-21, it is well known in the art to configure a mapper to map an input bits to a two constellation points in an encoder constellation table. Given that it would have been obvious to one skill in the art to configure the mapper of Betts et al to map the input bits to a two constellation points so as to satisfied desired system design requirements.

As per claim 3, note applicant acknowledges at page 19, lines 10-12 of the specification that the operation of a dual skipping switch is familiar to one skill in the art. Given that fact it would have been obvious to one skill in the art to configure the skipping switch in such a way to skip over 3 (bits) tones so as to satisfy desired interleaved depth.

As per claim 4 see claim 3.

As per claim 5, it would have been obvious to one skill in the art to set the non-sequential order as variable in order to increase system flexibility.

As per claim 6, it would have been obvious that the non-sequential order would have been dynamically determined by the receiver and the reason to do so would have been the same as provided above with respect to claim 5.

As per claim 7, see claim 3.

As per claim 8, it would have been obvious that the plurality of bits on tones would have been DMT symbols so as to be able to take advantages of advantage of DMT technological features.

As per claim 11, it would have been obvious to one skill in the art to set the encoder to a zero state prior to start of data frame in order to purge the encoder of any residual encoded signal from prior encoded frame.

12. Claims 9-10, 12-16 and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Betts et al US Patent No. 4,677,625 in view of Maloon et al US Patent No. 4,635,278 further in view of Voith et al US patent No. 5,751,741.

As claim 9, as applied to claim 1 above, Betts et al and Maloon et al discloses the invention substantially as claimed but does not explicitly teach a constellation buffer for receiving the convolutionally encoded plurality of bits from the synchronized switch. Voith teaches a constellation buffer 82 configured to store convolutional encoded data see fig. 4. Given that fact, it would have been obvious to one skill in the art to incorporate such a teaching in Betts et al and Maloon et al so as to avoid any data lost.

As per claim 10, see claim 9 and Voith further teaches an extractor buffer 70 for storing the plurality of bits prior to convolutional encoded the signal. See fig. 4 and the motivation to store the plurality of data bits prior to any encoding would have been the same as provided above with respect to claim 9.

As per claim 12, see claim 9.

As per claim 13, note that Betts et al further teaches a QAM encoder (mapper) that maps the inputs signal into a point of a preselected signal constellation see col. 2, lines 55-60. It fails to however teach that the mapper (QAM encoder maps the input bits to a two points constellation. As acknowledged by applicant at page 19, lines 20-21, it is well known in the art to configure a mapper to map an input bits to a two constellation points in an encoder constellation table. Given that it would have been obvious to one skill in the art to configure the mapper of Betts et al to map the input bits to a two constellation points so as to satisfied desired system design requirements.

As per claim 14, it would have been obvious to one skill in the art to set the non-sequential order as variable in order to increase system flexibility.

As per claim 15, it would have been obvious that the non-sequential order would have been dynamically determined by the receiver and the reason to do so would have been the same as provided above with respect to claim 14.

As per claim 16, it would have been obvious that the plurality of bits on tones would have been DMT symbols so as to be able to take advantages of advantage of DMT technological features.

As per claim 23, see claim 12.

As per claim 24, see claim 13.

As per claim 25, see claim 14.

As per claim 26, see claim 15.

As per claim 27, see claim 16.

13. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art fig. 4 in view of Rademeyer EP document no. 0673163A1.

Applicant's admitted prior art fig. 4 discloses an apparatus comprises an input see fig. 4, the input being two bits from a binary word; a plurality of logic gates 404; a plurality of unit time delays 402 for storing values based on previous inputs see fig. 4; an output including the input XU1 and U2 a third bit U0 based on the input (U1 and U2) the stored values see fig. 4 and the logic gates see fig. 4. However, Applicant's admitted prior art does not teach that the delays are set to zero prior to the start of each frame it also fail to teach that the delay is variable. However, setting the delays to zero prior to the start of any frame does not involve any inventive step, given that, it would have been obvious to one skill in the art to set the variable delays are set to zero prior to the

start of each frame in order to purge the apparatus of any residual encoded signal from prior encoded frame. In addition, configuring an encoder with a variable delay is old and well known in the art for instance Rademeyer teaches an encoder configured with a variable delay. Given that fact, it would have been obvious to one skill in the art to incorporate such a teaching in applicant's admitted prior art so as to enhance the performance of the encoder.

14. Claims 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Betts et al US Patent No. 4,677,625 in view of Hu et al US patent No. 5,841,819.

Betts et al discloses a transmitter (fig. 1), comprising: a limited plurality of inputs 14), a limited plurality of trellis encoder 18-24 for receiving a plurality of bits and for producing an output see fig. 1; (note that the trellis encoders are a type of convolutional encoder see for instance abstract, where convolutional decoder and trellis decoder are used interchangeably) and the output is based on unit time delays (28, 30 and 32) and logic gates (34 and 36) and the number of encoders (4) being equal to the limit on the plurality of inputs bits ((4) i.e X1, X2, X3 and X4) a synchronized dual switch (10, 16 and 42) configured to performed the following: connecting a first input to a first encoder and connect the output of the encoder to a mapper 44 (QAM encoder) ; connecting a second input to a second encoder and connect the output of the encoder to a mapper 44 (QAM encoder) ; connecting successive inputs to successive convolutional encoder and connect the output of the encoder to a mapper 44 (QAM encoder) until the limit is reached. However, Betts does not teach that the inputs are two bits of a binary word

derived from DMT symbol and it also fails to teach that the mapper is a coset mapper. It would have been obvious to one skill in the art to derive a two bits input from a DMT symbol so as to satisfy system requirements. In addition that the used of coset mapper is old and well known in the art for instance Patent No. 5,841,819 to Hu et al teaches the use of a coset mapper see fig. 2 and col. 4, lines 40-65. Given that fact, it would have been obvious to one skill in the art to use such a mapper in place of the QAM encoder (mapper) used by Betts so as to generate desired mapping signals consistent with design goal.

As per claim 29, it would have been obvious that the limit would have been variable so as to increase system flexibility.

As per claim 30, it would have been obvious that the variability would have been dynamically controlled by a receiver and the reason to do so would have been the same as provided above with respect to claim 29.

As per claim 31, it would have been obvious to one skill in the art to set the encoders to a zero state prior to start of data frame in order to purge the encoders of any residual encoded signal from previously encoded frame.

Allowable Subject Matter

15. Claims 17-22 are allowed.

Response to Arguments

16. Applicant's arguments, see response, filed on 11/15/04, with respect to the rejection(s) of claim(s) 1-31 under the section of 103 with respect to Laroia and Alcatel have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made as set forth below in view of Betts, Maloon and Voith. Note that the argument about the fact that Betts does not teach a synchronized dual skipping switch is not convincing as Betts clearly teach a switch functionally equivalent to the claimed synchronous skipping switch see art rejection above. The argument in reference to the used of a coset mapper is moot in view of the new ground of rejection set forth above.
The art rejection of claim 17 and related dependent claims is withdrawn because the art of record does not explicitly teach the limitations recited in steps a and b.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Corrielus whose telephone number is 571-272-3020. The examiner can normally be reached on Maxi-Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean B Corrielus
Primary Examiner
Art Unit 2637
10-28-05